applied sciences

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Distributed Generation Control Using Modified PLL Based on Proportional-Resonant Controller

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Received: 4 November 2020; Accepted: 10 December 2020; Published: 12 December 2020

Abstract: Due to the increasing necessity for electrical demand, the microgrids (MGs) based on distributed generations (DGs) within power electronic interfaces are being extended to improve the traditional network control. One of the common ways to achieve power sharing among the resources on an islanding MG is to use the droop control approach, performing based on proportional-integrator (PI) controllers. However, due to the effect of feeder impedance, obtaining the reactive power sharing using this method is not accurate and leads to overload in some DGs, resulting in the output terminal voltage of each DG going outside of the allowable range. The second problem arises when the frequency measurement is not performed precisely, leading to inaccurate active power sharing, which can be solved by using an improved phase locked loop (PLL). Therefore, the purpose of this paper is to propose an applicable and simple approach based on the use of conventional droop characteristics and a proportional-resonant (PR) controller in a DG control system. Due to the load changes in the microgrid and other contingencies, the proposed PLL-based controller is able to represent supreme performance with low error in several case studies.

Keywords: controller; distributed generation; modified proportional-integrator; PLL; power systems; proportional-resonant controller

1. Introduction

In recent years, distributed generation (DG) units under smart grid ambient and assisted by a cyber-physical system have been considered in microgrids (MGs) [1–4] to attain some benefits such as supplying the local loads, increasing reliability, reducing greenhouse gases, and delivering power to low voltage networks. To overcome the technical problems of connecting the DGs to the upstream distribution network, the concept of MGs have come to the attention of researchers, which are several collections of DGs, energy storage systems (ESSs), and loads which are responsive or not, as shown in Figure 1. A MG may be operated in grid connected mode or islanding mode due to a fault occurrence, maintenance scheduling, or maybe normal condition [5–7]. The voltage/frequency stability and optimal power management of DGs are the two significant concerns while providing the demand loads. In order to make sure that the most stable situations are obtained, an applicable control approach should be employed to make the renewable energy sources (RESs) not be overloaded [8].

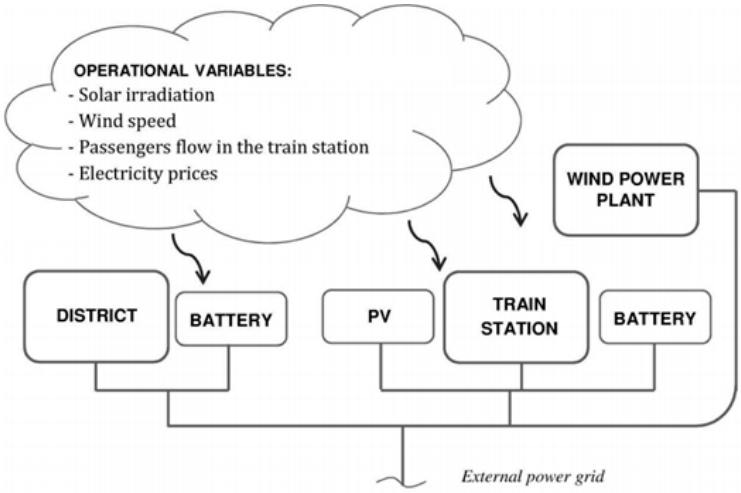


Figure 1. A typical microgrid (MG) considering distributed generations (DGs).

One of the common approaches of power sharing among DGs in an island MG is frequency-active power (f-P) and voltage-reactive power (E-Q) characteristics of the drop control method. The drop controllers improve the performance of the DGs by proportionally sharing the power for the resources and reducing the rotational current among them. Due to the universality of frequency quantity, the sharing of active power among the sources is done accurately, however for reasons such as the pairing between real and reactive power, the limitation of voltage variations, and the dependence of reactive power on grid parameters, such as feeder impedance, conventional drop control is unable to properly distribute reactive power among DGs, resulting in overload of some resources. In addition to sharing reactive power, adjusting the acceptable voltage profile for consumers is also a particular importance [9–11]. There are several techniques that have been proposed to improve the droop characteristic of parallel inverters such as semi-centralized control [12], adaptive voltage characteristic [13], virtual frame [14], signal injection [15], and virtual impedance [16]. In [16], in order to achieve proper load sharing and reduction of circulating current for different line impedances, the concept of virtual impedance along with single-cycle control has been utilized.

The "reactive power based on voltage derivation" feature to improve the reactive power sharing is presented in [17]. Although the use of this method reduces the reactive power sharing errors, it does not guarantee the ideal reactive power sharing for sources. Furthermore, the improvement of reactive power sharing is not evaluated considering the local load. A method for modifying the E-Q characteristic is presented in [17] with the aim of achieving the ideal reactive power sharing in a MG with an arbitrary structure and DGs considering local control. The reactive power sharing error is eliminated at specific times and by performing a special process while correcting the bandwidth from the E-Q characteristics of various sources. In order to achieve the desired result, all the resources in the MG have to perform the process simultaneously, and a low-bandwidth communication channel is used among the sources. Although the proposed scheme is one of the few methods for which no special constraints are considered on the network, the characteristic correction process in this way is a procedure with inappropriate dynamics with severe fluctuations in the output of DGs. In [18], the real power can be controlled directly by the voltage variations and the reactive power is dependent to the frequency. Therefore, in resistive MGs, the inverse E-P and ω-Q characteristics can be used to weaken the coupling between active and reactive powers to maintain system stability. The dynamic response is as desirable as possible, while the E-P characteristic is still of the drop type, and due to the inverse relationship between reactive power and frequency, the ω-Q characteristic must be of the incremental type [17].

Using a predetermined virtual inductor and estimating the feeder impedance, the slope of the voltage droop characteristic is corrected to compensate the voltage fluctuations across the feeder impedance variation [18]. Nevertheless, to estimate the feeder impedance, it is necessary that the

MG be operated in grid connected mode before operating in the islanding mode. In [19], the point of common coupling (PCC) voltage harmonics is measured and sent via a telecommunication link to the local controller (LC) of each DG to estimate the feeder impedance. This estimation is based on the assumption of a small difference in the phase angles difference between the source voltage and the PCC voltage. Through measuring the feeder current, the authors in [20] presented an approach to estimate the feeder impedance. It is worth noting that there are many methods in grid control considering the parallel inverters, but they use complicated calculations to determine the control loop coefficients such as fuzzy [21], artificial neural network (ANN) [22], sliding mode control (SMC) or combined with space vector modulation [23,24], multi agent [25], hierarchical process [26], and master slave techniques [27].

Phase locked loops (PLLs) have many applications in the field of power engineering to detect the operation frequency. In cases where the synchronous operation of a converter is required, the most common method is to use PLL. However, network disturbances due to noise, unbalancing, and harmonics can impair the performance of a PLL and the system connected to it [28–30]. PLLs are found in modulators, de-modulators, state-of-the-art frequency suppliers, and a variety of signal processes. The PLL mechanism is described as follows: if the input signal is not equal to the internal oscillator signal, the amplified phase error signal causes the voltage controlled oscillator (VCO) frequency to deviate from the input signal direction. Under proper conditions, the VCO signal completely locks in the input signal. Note that the output signal of phase detector is DC and the control input of VCO has some frequency harmonics with it. The output of VCO should be a signal with a generated frequency equal to the input. Therefore, it is somewhat difficult to detect and clean the input from noise. Because any slight variation in the potential difference of the circuit will cause a frequency shift, and the VCO output can compare and lock a triangular, sine wave, or whatever noise which is generated by the operation method. Consequently, the noise will appear in the PLL outputs [31,32]. In order to avoid observing these malfunctions, an appropriate scheme is proposed in this paper based on classic stationary frame and Clarke transformation.

The novelties of presented paper are mentioned in bullet below:

- A modified proportional-resonant (PR) controller is proposed to overcome reactive power sharing errors considering feeder impedance effect. This leads to a more simple implementation than other complicated approaches.
- Some modifications are applied to the conventional PLLs to develop the performance. This can help us to detect phase shift and harmonic compensation.
- The simplicity of proposed method has raised the accuracy and system response in each case study. This causes low overshoot and minimized settling time.

This paper is organized as follows: in Section 2, the existing PLLs are described and the modified PLL is proposed. Section 3 describes the proposed PLL validation using some control indices such as settling time and overshoot considering some case studies. The system under study with PR controller and problem formulation are presented in Section 4. In Sections 5 and 6, the simulation results and discussion are presented, respectively. Finally, in Section 7, the conclusion is expressed.

2. Modified PLL

The proposed PLL functions based on a moving average filter (MAF) and enhancement of performance (EP) block. In this way, the problems of offset fault, difficult tuning, sluggish dynamic response of the conventional PLLs, and even the harmonics compensation are overcome. In EP-MAF-PLLs, a pre-filtering block is hired to shift the MAF phase angle to a certain value, and then, there is a phase shift from the phase detector section, resulting in eliminating the system errors and enhancing the transient system response. Furthermore, an improvement is applied to the rotating speed of synchronous reference frame (SRF or dq frame) to retrieve an appropriate tuning calculation and remove the harmful effects of offset errors. The EP-MAF-PLL exhibits the dq-PLL phase angle extraction algorithm as well as other approaches. The only malfunction of EP-MAF-PLL is that

it needs high frequency performance and phase angle overshoot at the time of fault, because of the defective algorithm used in phase extraction process.

These above-mentioned difficulties have motivated the authors to develop a novel PLL named stationary frame EP-MAF-PLL (SF-EP-MAF-PLL), which is the mixture of EP-MAF-PLL and the classic αβ-PLL. The projected SF-EP-MAF-PLL is able to diminish the frequency overshoots by receiving the subordinate frequency overshoot property of the classic αβ-PLL. Moreover, the proposed PLL leads to precise phase angle extraction because of the improvement assimilated for phase offset errors, similar to conventional EP-MAF-PLL. Therefore, SF-EP-MAF-PLL empowers the speedy operation of grid side converter under grid faults by keeping the frequency in permissible range.

The block diagram of MAF-PLL is represented in Figure 2, which shows a slow dynamic response due to the attendance of MAF in the control loop. The closed loop transfer function consequences in 4th order system, for which the tuning procedure is complex and relies on a symmetrical technique. This slow dynamic response of MAF-PLL is mostly because of the settling time (ST) that has been chosen on the lower band limit. In [33], an approach is proposed that proves the ST should not be less than 25 ms, results in decreasing phase margin (PM) and exceeding the system instability. In addition, a large offset error is observed for operation in all frequency spectrums, but the fundamental. These drawbacks could not be ignored in sensitive applications.

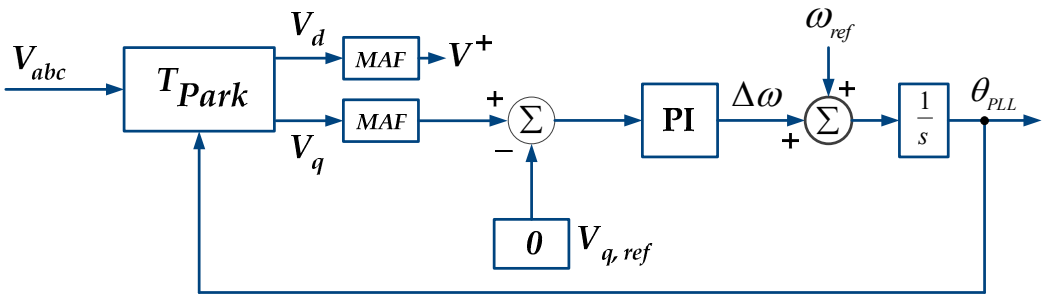


Figure 2. The moving average filter-phase locked loop (MAF-PLL) structure.

In EP-MAF-PLL, a new algorithm is recommended to solve the problems of slow dynamic response, using a pre-filtering stage as shown in Figure 3. The error appeared under off-nominal operation frequency is moderated in this structure. However, in unbalanced conditions, this PLL is not able to mitigate the frequency overshoots caused at the fault happening moments [34,35].

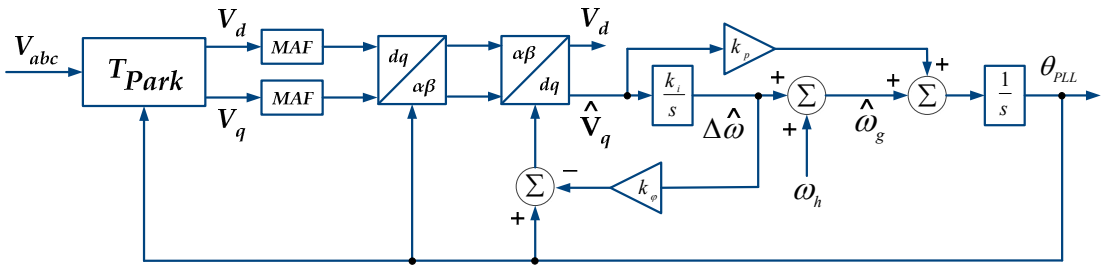


Figure 3. The enhancement of performance (EP)-MAF-PLL structure.

In order to compensate the frequency overshoots, the authors added a new phase detector section to the EP-MAF-PLL structures, which is the proposed strategy of this paper. In classic αβ-PLL structure, lower frequency overshoot could be decreased while the phase angle overshoot is varied around the set point. An estimation used to obtain the phase angle in low values, could be mathematically represented:

$$\Delta\theta = \theta_{AC} - \theta_{PLL}$$
$$if : (\Delta\theta \to 0) \Rightarrow \begin{cases} \sin(\Delta\theta) \sim \Delta\theta \\ \cos(\Delta\theta) \sim 1.0 \end{cases} \quad (1)$$

Using trigonometric ratios result in:

$$\Delta\theta \sim \sin(\Delta\theta) = \sin(\theta_{AC} - \theta_{PLL}) = \sin(\theta_{AC})\cos(\theta_{PLL}) - \sin(\theta_{PLL})\cos(\theta_{AC}) \quad (2)$$

This improvement to classic αβ-PLL leads to compensate the phase angle error observed due to off nominal frequencies, before. The proposed PLL named SF-EP-MAF-PLL is represented in Figure 4, considering $\Delta\theta$ estimation.

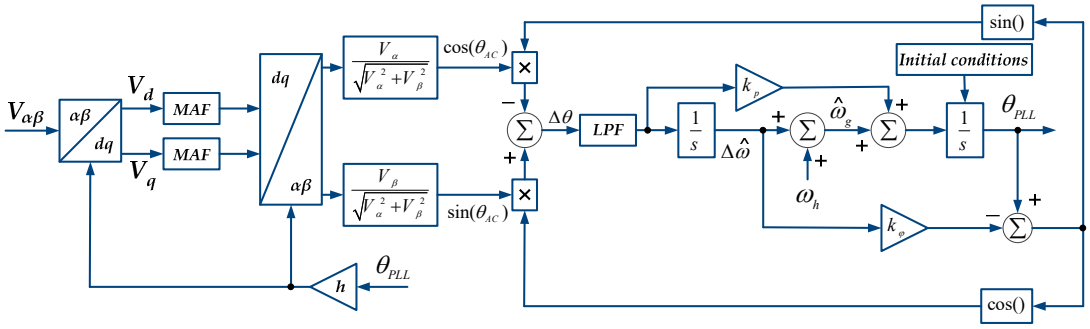


Figure 4. The proposed stationary frame (SF)-EP-MAF-PLL structure.

3. Proposed PLL Validation

In order to validate the performance of the SF-EP-MAF-PLL, three case studies using Matlab/Simulink were investigated on a basic and sample microgrid [36]. The tuning coefficients are represented in Table 1 for both EP-MAF-PLL and SF-EP-MAF-PLL structures. There are different ST values to determine the system dynamic response, which are slow (4 times of a period where T = 20 ms), medium (3T) and fast (2T), while the simulations are carried out with medium ST conditions.

Table 1. Tuning coefficients based on settling time (ST) variations.

Settling Time	SF-EP-MAF-PLL	EP-MAF-PLL
	k_p	k_p
4T	905.71	544.32
3T	1125.42	700.12
2T	4983.15	3214.56

3.1. Normal Conditions

In normal conditions, it is expected that the PLLs work properly to detect the system frequency; however, as shown in Figure 5, the SF-EP-MAF-PLL has better rise time and overshoot compared with the EP-MAF-PLL structure.

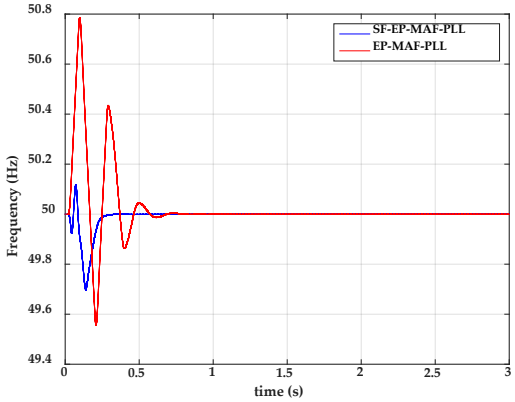


Figure 5. The frequency measured using two kinds of PLL in normal condition.

3.2. Load Change

At this stage, in order to evaluate the performance of the PLLs, it was assumed that the system load doubles at t = 1 s and returns to normal condition at t = 2 s. It was expected that during the transient moments, the network frequency would be slightly disturbed and would return to normal quickly. Figure 6 shows the frequency detection behavior for both PLLs. It is clear that the traditional PLL shows higher overshoots than the improved one.

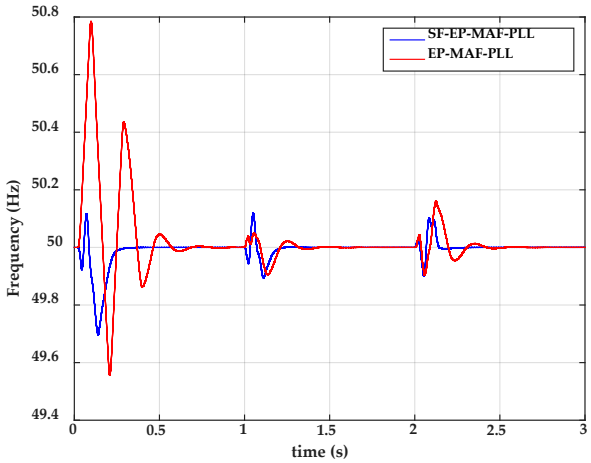


Figure 6. The frequency measured using two kinds of PLL in load variation condition.

3.3. LG Short Circuit Fault

In this case study, a single-phase line to ground fault occurred at t = 1 s and cleared at t = 2 s. Due to the fact that the amplitude of the perturbation is greater than the previous, it is expected that higher overshoots will also be observed at the output of the PLLs. At the same time, the behavior of SF-EP-MAF-PLL was more appropriate than EP-MAF-PLL, since it resulted in fewer overshoots and faster response speed as shown in Figure 7.

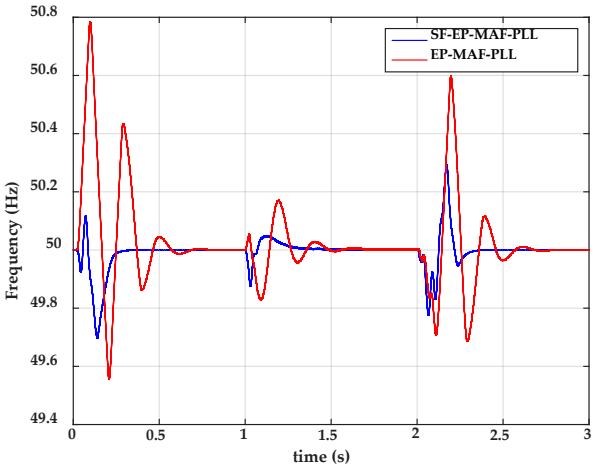


Figure 7. The frequency measured using two kinds of PLL in fault condition.

4. System under Study with PR Controller

A simplified DG under consideration is represented in Figure 8 to show the DC link voltage, inverters, the Park or Clarke transformations, and the local load, in a three phase structure.

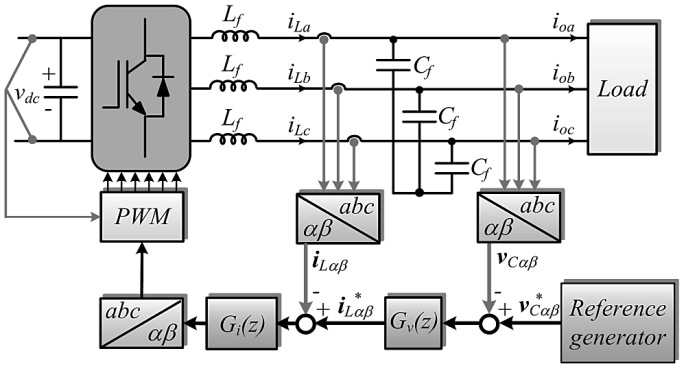


Figure 8. A sample DG and RLC filter feeding a load.

In this situation, the demonstration in the discrete-time domain is based on the Z-transformation associated to the inductor current $G_p(s)$ along with the sample and hold effect [37], which is given by:

$$G_p(z) = \frac{I_{L\alpha\beta}}{V_{i\alpha\beta}} = \left(1 - z^{-1}\right) Z\left\{\frac{G_P(s)}{s}\right\} = \frac{1}{R_f} \frac{\left(1 - e^{-\frac{T_s}{\tau_p}}\right) z^{-1}}{1 - e^{-\frac{T_s}{\tau_p}} z^{-1}} \tag{3}$$

where $I_{L\alpha\beta}$ and $V_{i\alpha\beta}$ are the inductor current and input voltage in the z-domain, respectively, and $\tau_p = L_f/R_f$ is the plant time-constant. The state space equations of system are mathematically formulated by:

$$\begin{aligned} \frac{d}{dt} v_c(t) &= \frac{1}{C_f} i_L(t) \\ \frac{d}{dt} i_L(t) &= \frac{1}{L_f} (v_i(t) - R\, i_L(t) - v_c(t)) \end{aligned} \tag{4}$$

If the expressed in Equation (4) are transformed to the Laplace domain including the effects of initial conditions, we could re-write by:

$$\begin{aligned} V_c(s) &= \frac{\omega_n^2}{s^2 + 2\zeta\omega_n + \omega_n^2} \Theta(s) \\ \Theta(s) &= \frac{v_i(t=0)}{s} + \frac{s v_C(t=0) + \dot{v}_c(t=0)}{\omega_n^2} \end{aligned} \tag{5}$$

$$\begin{aligned} I_L(s) &= \frac{\omega_n^2}{s^2 + 2\zeta\omega_n + \omega_n^2} \Lambda(s) \\ \Lambda(s) &= C_f v_i(t=0) + L_f C_f s i_L(t=0) - C_f v_c(t=0) \end{aligned} \tag{6}$$

where:

$$\begin{aligned} \zeta &= \frac{1}{2\omega_n} \frac{R_f}{L_f} \\ \omega_n^2 &= \frac{1}{L_f C_f} \end{aligned} \tag{7}$$

where ω_n is the natural frequency of the system and ζ represents the damping factor. To determine the reference current and voltage for the voltage source inverter (VSI), according to Figure 8:

$$\begin{aligned} i^*_{L\alpha\beta} &= \left(v^*_{C\alpha\beta} - v_{C\alpha\beta}\right) G_v(z) \\ gate_{pulses} &= \left(i^*_{C\alpha\beta} - i_{C\alpha\beta}\right) G_i(z) \end{aligned} \tag{8}$$

where $G_v(z)$ and $G_i(z)$ are given by:

$$\begin{aligned} G_v(z) &= k_{P(v)_h} + \frac{k_{R(v)_h} z^{-2}}{1 - C_h z^{-2}} \\ G_i(z) &= k_{P(i)_h} + k_{R(i)_h} \frac{z^{-1}\cos\left(h\omega_1 T_s + \phi'_h\right) - z^{-2}\cos\left(\phi'_h\right)}{1 - 2z^{-1}\left(1 - C_h \frac{T_s^2}{2}\right) + z^{-2}} \end{aligned} \tag{9}$$

where T_s is the sampling time and C_h is given by:

$$C_h = 2 \sum_{n=1}^{N_{T_s}/2} \frac{(-1)^{n+1} h^{2n} \omega_1^{2n} T_s^{(2n-2)}}{(2n)!} \tag{10}$$

Stability Analysis

In order to evaluate the stability analysis, root locus diagram and Nyquist curves are presented in Figures 9 and 10. It can be established from Figure 9 that the poles of the open-loop system are all located on the left side of the imaginary axis. Moreover, the system is minimum-phase and no zeroes are seen on the right side of the $j\,\omega$ axis. Figure 10 shows that the Nyquist diagram does not revolve around point $-1 + j\,0$ pu and hence: $N = 0$. Furthermore, since the open-loop system has no poles on the right side of the imaginary axis, we have: $P = 0$. Now, according to control and stability principles in calculation the residuals by "Cauchy–Euler" integral and revolving clockwise, $Z = N + P = 0$ is obtained. As a result, the closed-loop system is permanently stable.

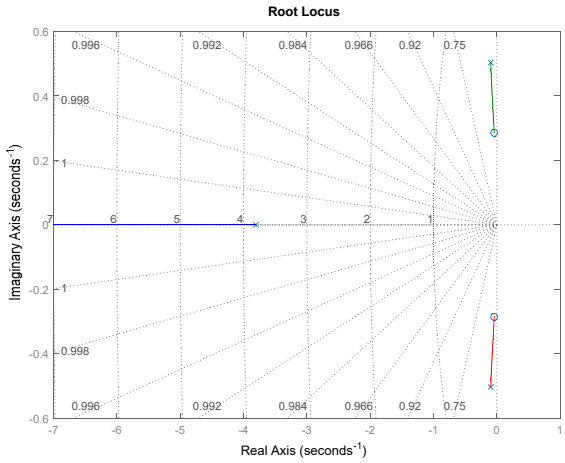


Figure 9. Root locus diagram of the control system roots.

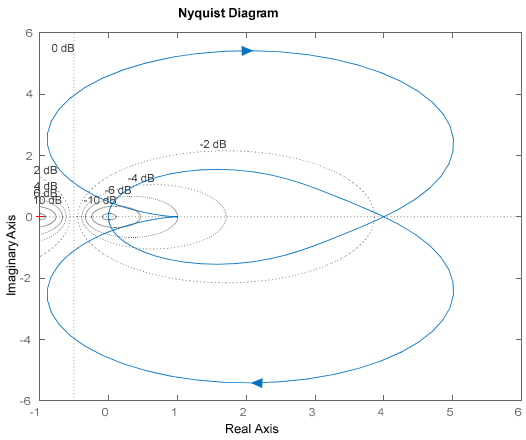


Figure 10. Nyquist diagram of the control system roots.

5. Simulation Results

To verify the proposed control system, four case studies were conducted on a MG with characteristics given in Table 2. In these case studies, the effect of load fluctuation, interconnection of sources, entrance and exit of the DGs, connection to and disconnection from the upstream network, unbalancing, etc. were reviewed and analyzed.

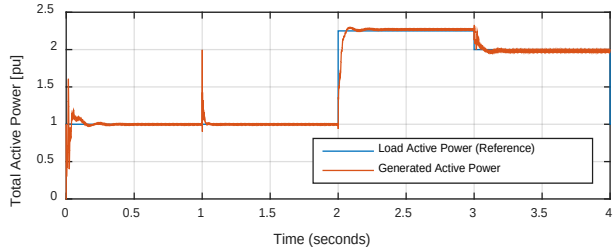
Table 2. System specifications.

Parameter	Value
AC grid voltage (V_{AC})	380 Vrms
AC grid frequency (f_{AC})	50 Hz
Switching frequency (f_{sw})	12 kHz
Filter resistance (R_f)	10 mΩ
Filter inductance (L_f)	1.8 mH
Filter capacitance (L_f)	470 μF

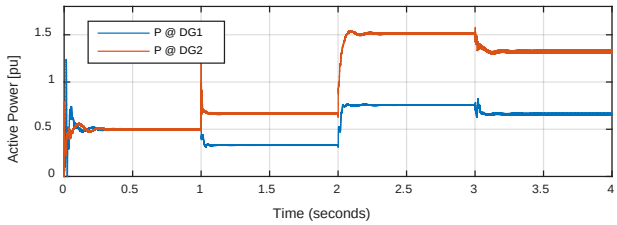
5.1. First Case Study

Suppose the MG working in the islanding operation and the load demanded is $1 + j\,0.7$ pu. If the capacity of DG_2 is twice as big as the capacity of DG_1, it is expected that the power extracted from DG_2 is twice as big as the one from DG_1. This means DG_2 supplies 0.67 pu and DG_1 supplies 0.33 load. If DG_2 consists of two similar units, it is supposed that until t = 1 s, only one unit of DG_2 and full capacity of DG_1 is perched in the circuit. Therefore, active and reactive powers distribute between them optimally and equally. Then, at t = 1 s both units of DG_2 perch in the circuit and it operates with full capacity. Therefore, as explained before, DG_2 supplies load, twice as much as DG_1 does. This situation continues to hold until t = 2 s. By this time, $1.25 + j\,0.6$ pu load is added to the existing one in the circuit and power distribution continues as the previous state. At the time t = 3 s, another load fluctuation happens and due to necessity of frequency and voltage control, active load decreases by j 0.25 pu and reactive load increases by j 0.55 pu. Active and reactive powers of DG units and frequency control diagrams are shown in Figures 11 and 12.

The sum of total active and reactive powers is shown in Figure 11a,b. Clearly, the proposed controller has been able to track the reference signal properly. Figure 11c,d illustrate active and reactive powers of the source. From Figure 12a, it can be observed that at load fluctuation time, frequency has low swing, but it returns to its final and steady value. Figure 12b,c illustrates the voltages of these sources in dq frame. Stability of d-axis voltage and q-axis voltage remaining at zero suggest the proper performance of the controller.



(**a**)



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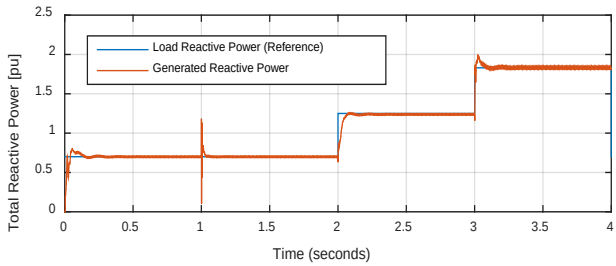

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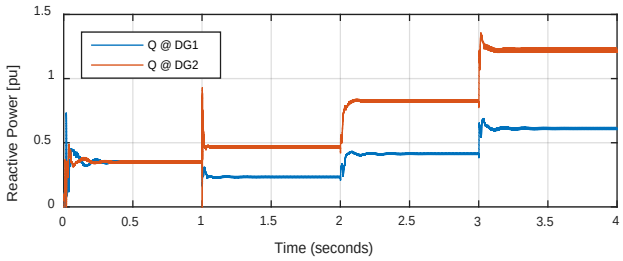


(**d**)

Figure 11. First case study results: (**a**), total active power of load; (**b**), produced total active power share of sources; (**c**), total reactive power of load; (**d**), produced reactive power share of source.

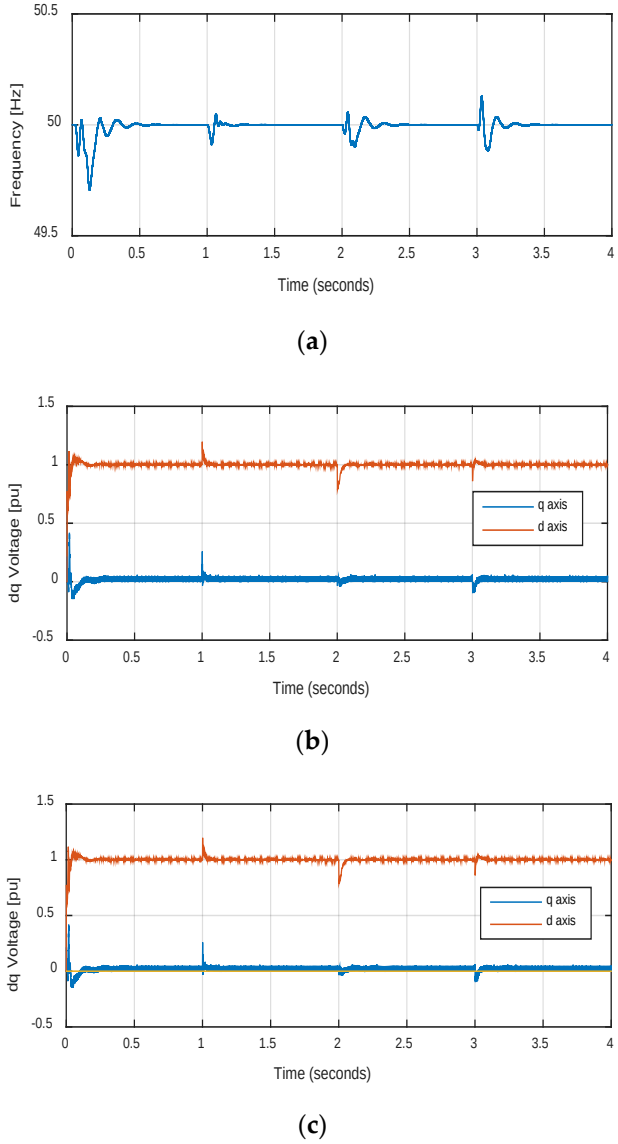


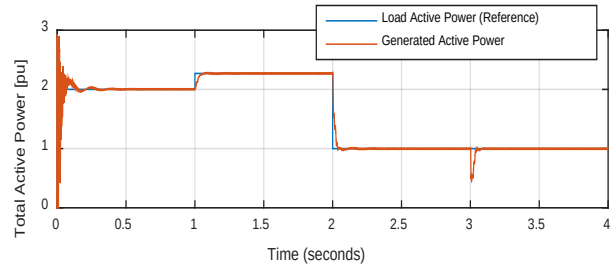
Figure 12. main parameters in the first case study; (**a**) Network frequency, (**b**) the voltage of the DG_1 source, (**c**) and the voltage of the DG_2 source.

5.2. Second Case Study

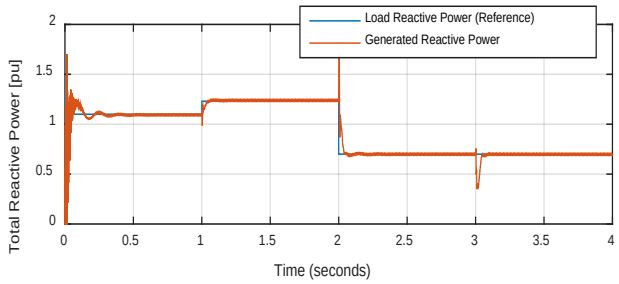
In this case, we supposed that the MG under study was connected to the upstream network until $t = 1$ s and then disconnected from it due to safety issues. Therefore, from $t = 1$ s onwards, it will work in islanding operation mode, and power distribution is conducted in accordance with the former situation, in 2-to-1 proportion. When the MG is connected to the upstream network, it is supposed that the power received from the upstream network is only reachable up to $3 + j\,0.12$ pu. In other words, reference current of the upstream network is restricted to the mentioned value, so that utilizing the downstream for satisfying load demands would be possible. This also helps with improving the efficiency of the DGs. After $t = 1$ s, the DGs of the micro grid distribute the load in a 2-to-1 proportion among themselves and this trend continues until $t = 3$ s, and even after an intense decrease of load, by $1.2 + j\,0.6$ pu at $t = 2$ s. At $t = 3$ s, the production unit number 2 leaves the circuit completely. Therefore, all load supply responsibility will be on the DG number 1.

As it can be seen in Figure 13, after $t = 3$ s until the end of the simulation, the total amount of load is equal to active and reactive powers production of source number 1. Furthermore, in Figure 13b,c, the upstream network and active and reactive powers of scattered production sources are illustrated.

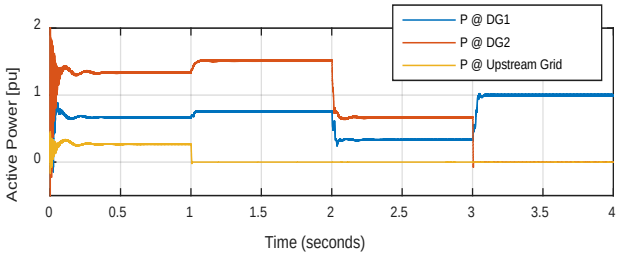
Optimum power distribution among sources with certain proportions can be figured out by comparing Figure 13b with Figure 13c.



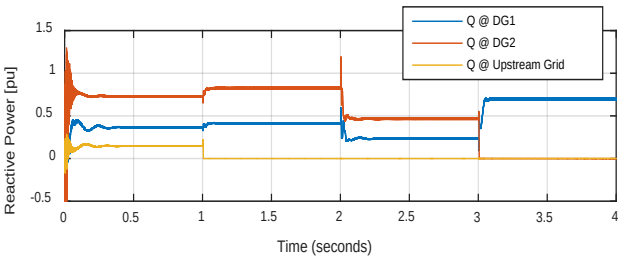
(**a**)



(**b**)



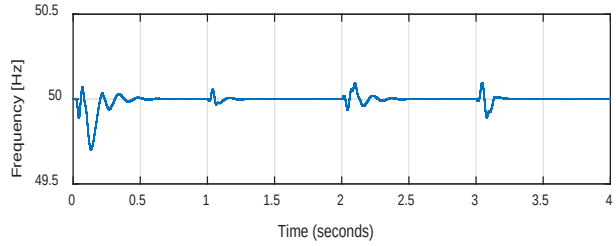
(**c**)



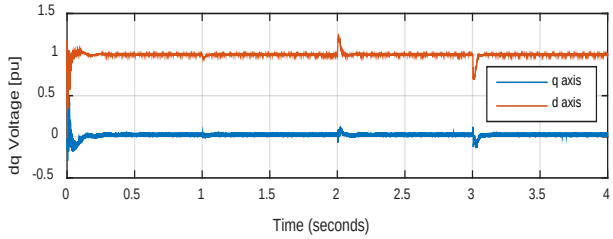
(**d**)

Figure 13. Second case study results: (**a**), total active power of load; (**b**), produced total active power share of sources; (**c**), total reactive power of load; (**d**); produced reactive power share of source.

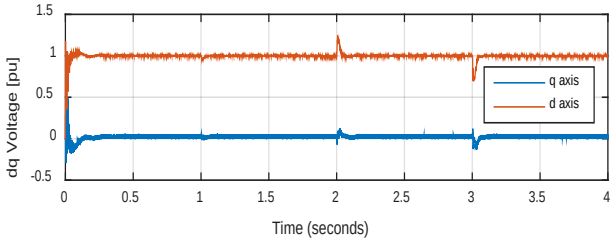
In Figure 14a, the network frequency after the happenings mentioned previously is shown. It can be seen that the primary fluctuations dampen at most after 0.2 s and the steady state error becomes zero. Figure 14b,c show voltage diagrams of *dq* frame for DG indices 1 and 2.



(**a**)



(**b**)



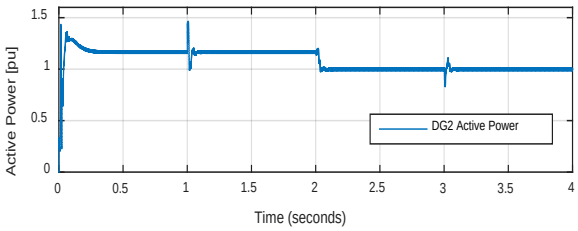
(**c**)

Figure 14. Network frequency (**a**), the voltage of source DG_1 (**b**), the voltage of source DG_2 (**c**) in the second case study.

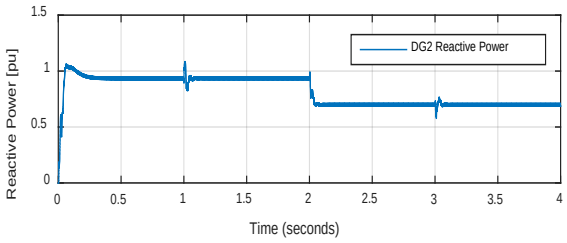
5.3. Third Case Study

The effect of feeder impedance on controlling the network is studied in this section. Suppose that the serial branch of the feeder impedance is available in accordance with Table 2. In this case, only 1 digit is in the circuit and supplies the load. At $t = 1$ s, a serial RL branch, similar to what is used in the output of the inverter, connects to the previous branch in parallel. As a result, the impedance of the RL sum branch is halved. It can be observed from diagrams in Figure 11 that not only is there no change in the produced power of the DG unit, but also the circuit frequency only undergoes few fluctuations in high frequencies and goes back to the stable state. Now, with the new filter impedance, at $t = 2$ s load decreases by $0.2 + j\,0.3$ pu. In spite of fluctuation in filter impedance, frequency quickly stabilizes on 50 Hz and the transient error becomes critically damp and power distribution is conducted.

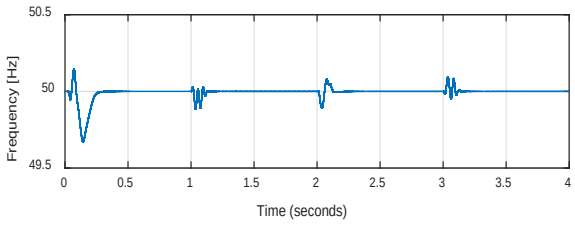
At $t = 3$ s, the new filter impedance branch disconnects from the circuit, so that the network goes back to its previous state. It can be seen that frequency and power fluctuation dampens after 0.08 s, and stability at the former quiescent point, returns to the system. Figure 15a–d show the output active and reactive powers of DG and its frequency and voltage diagrams, respectively.



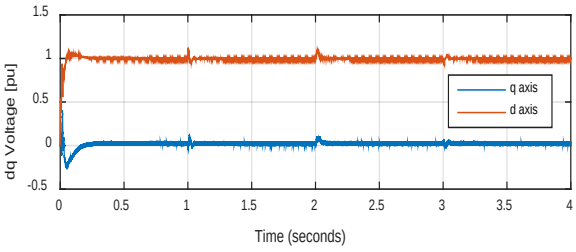
(**a**)



(**b**)



(**c**)



(**d**)

Figure 15. Third case study results: (**a**), active power of load; (**b**), reactive power of load; (**c**), network frequency; (**d**), load voltage.

5.4. Unbalancing, LG Fault, Feeder Impedance, and Load Variation

In this case study, the unbalancing load condition is discussed. Therefore, the DGs should participate in the unbalancing with the algorithm below:

(a) If the unbalancing is procurable only with one DG, the DGs must supply the unbalanced current from low capacity to high capacity one by one.
(b) If there are any single phase DGs which could have supplied the defective phases, the corresponded DG must procure the unbalanced load located at this power line.
(c) If there are grid-connected operation modes, since the DGs cannot supply the unbalanced current, the up-stream network participates in the condition.

According to the management algorithm above, this case study is conducted with a three-phase unbalancing load. From the beginning to t = 2 s, a three-phase unbalanced load is connected to the system while at t = 1 s, the feeder impedance is changed as similar to case study 3 (Section 5.3).

At $t = 2$ s to $t = 3$ s, the unbalanced load is disconnected from the grid and the balanced system is obtained. Meanwhile, at $t = 4$ s to $t = 5$ s, a single-phase fault at phase A happens in order to examine the proposed controller stability. Then, at $t = 4$ s, the fault is cleared and the system is restored to its balanced condition. Figure 12 shows the *dq* voltage and current of the DG and the active and reactive power sharing. As represented in Figure 16d, the frequency is stable in all contingencies.

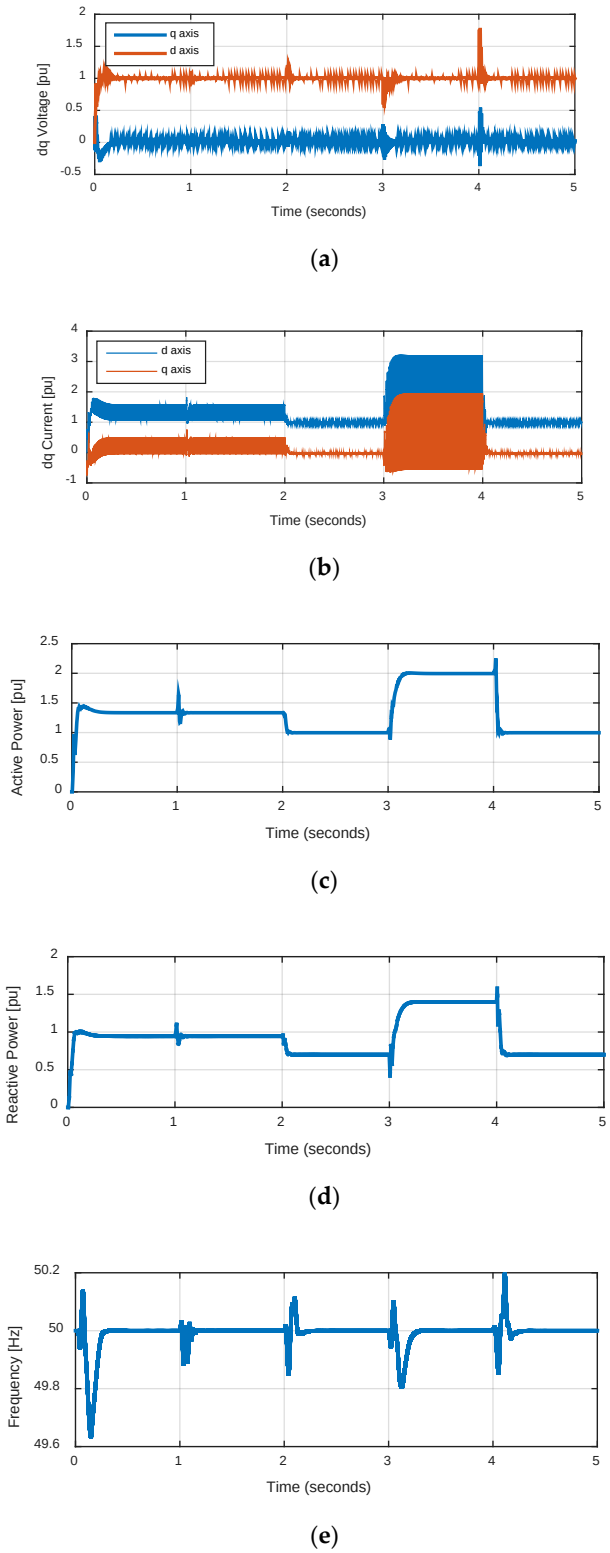


Figure 16. (**a**) *dq* voltage of DG output terminal; (**b**) *dq* generated current of DG; (**c**) generated active power; (**d**) generated reactive power; (**e**) system frequency.

6. Discussion

In this section, some PLLs have been compared in terms of processing time, frequency overshoot, and performance capability. Table 3 represents the results as below:

- The computational complexity of proposed PLL is lower than the others, which causes higher system response speed.
- The frequency overshoot of proposed PLL is lower than the others, which makes the more accurate solution obtainable.
- The processing time of proposed PLL is not the least in all PLL models, however, it is less than two of them.
- The DC offset can be considered in the proposed PLL, which will increase the system reliability.
- The harmonics effects could be implemented in the proposed PLL to raise the recovering performance. The minimum THD represent the lowest THD that is measured using a RL diode-bridge load.

Table 3. The comparison of modern PLLs.

PLL Type	Computational Complexity	Frequency Overshoot	Processing Time (ms)	Performance Capability	
				DC Offset	Harmonics (Minimum THD)
αβ-PLL	Low	Low	3.14	No	No (4.18%)
dq-SRF-PLL	High	High	8.91	No	No (4.11%)
MAF-PLL	Low	Low	2.93	Yes	Yes (3.78%)
EP-MAF-PLL	Low	High	4.62	Yes	Yes (3.13%)
SF-EP-MAF-PLL	Low	Low	4.33	Yes	Yes (1.10%)

7. Conclusions

In this paper, the improved power sharing among inverter based DGs in an island microgrid considering a PR controller is presented to minimize the terminal voltage error adjustment. In order to modify the frequency measured results, the SF-EP-MAF-PLL is proposed, which, compared with the other PLL models, has lower overshoot and a shorter processing time with harmonics compensation capability. The system stability, which has been checked by locus diagram and Nyquist theorem, guarantees the instability compensations. In load changing conditions, the proposed PLL has the lower overshoot by about 26% than the conventional EP-MAF-PLL, however, this improvement has been presented significantly as about 42% in short circuit faults. The output results obtained from various case studies carried out indicate the improvement in the performance of the proposed discrete PR controller and the frequency converges around its reference value.

Author Contributions: A.Z.: Conceptualization and methodology; M.M.: software and validation; R.M.: review and editing. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Conflicts of Interest: The authors declare no conflict of interest.

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